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# SMART Traffic Control System Designed Using Verilog HDL

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***Abstract***

**Background/Objectives:** Vehicular traffic is endlessly increasing everywhere that cause terrible traffic congestion on intersections. **Methods/Statistical analysis:** In this paper, the proponents brought the design of the traffic control system to mitigate this kind of setup. The central concept is to allow vehicles based on the first-in-first-out principle. Exceptional cases for emergency vehicle detection will be also introduced in order for the ambulance to reach its destination faster and effectively. The phases inclusive for this research are formulated Verilog source code, testbench modeling, simulation process via ISIM, and methodological stuff. The whole process has been synthesized and verified successfully. **Findings:** proposed system was designed through Verilog Hardware Description Language using the Xilinx ISE Design Suite 14.5 as for the primary software. **Improvements/Applications:** The proposed system allows emergency vehicles to pass along traffic and prioritizes the vehicles according to the first-in-first-out principle.

***Index Terms***

Emergency vehicle, First-in-first-out, Traffic control system, Verilog, Xilinx ISE

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## I. INTRODUCTION

Nowadays, traffic jamming was considered as one of the constant problem faced by metropolises and highly urbanized cities. Due to public transportation reliability issues, the demand for car arises but leaves a negative impact on the exhaustion of popular roads. To ease the problem regarding this matter, the government conducted several projects involving road widening and infrastructure program which could accommodate massive vehicle on public roads. But because of continuous urbanization and lack of long term solution to traffic, public roads cannot cater a large volume of vehicles. In addition, many people arrive in their respective workplace late. Thus, it also resulted to economic loss and inefficiency of businesses and industrial companies invested in our country. To address this emerging difficulty, the proponents designed and innovate a system which can reduce traffic congestion through the use of Verilog Hardware Description Language.

With the proposed system, the conventional fixed timing sequence of most traffic light will be replaced by using the first-in-first-out principle. It is capable of analyzing road direction to be prioritized based on who firstly arrived on intersection. On the other hand, human lives can be rush immediately to the nearest hospital. For this proposal, emergency vehicle like ambulance can be treated with the highest priority. (Swetha, et.al., 2017).

### *A. Objectives of the Study*

The main objective of this study is to innovate a system that can alleviate problems regarding traffic on intersection using Verilog HDL. The goal is to create a system that will help manage the traffic movement and to achieve maximum utilization of the four roads.

Specifically, this study also aims to provide simulations for the following situations:

1. A system that will allow the emergency vehicle to pass along the traffic.
2. A system that will prioritize vehicle according to the first-in-first-out principle.

## II. LITERATURE REVIEW

Junchen Jin and Xiaoliang Ma (2017) proposed a group-based signal control approach adept of constructing assessments based on its understanding of traffic situations at the intersection roads. The proposed system is selected to be matched with the prevalent signal scheme. Simulation results have shown that the control system outstrips the optimized GBVA control system primarily because of that's real-time adaptive learning capability in response to the fluctuations in traffic claim.

Nasser R. Sabar et al (2017) organized the undertaking of traffic on urban streets by unwavering the appropriate signal timing settings. The proposed algorithm was based on the memetic algorithm. The proposed algorithm was coded in the commercial microscopic traffic simulator, AIMSUN. The results demonstrated that the proposed algorithm was better than genetic algorithms and fixed-time sets.

Huajun Chai et al (2019) took the collaboration between travelers' route choice and traffic signal mechanism in a intelligible structure. They tested their algorithm and control strategy by simulation in OmNet++ (A network communication simulator) and SUMO (Simulation of Urban Mobility) under numerous circumstances. The simulation results revealed that with the proposed vigorous routing, the global travel cost expressively reduced.

Ishant Sharma and Dr. Pardeep K. Gupta (2015) proposed to replace existed traffic signals with a system that are monitored the traffic flow automatically in traffic signal and sensors are fixed in which so the time feed are made dynamic and automatic by processed the live detection.

Chandrasekhar.M et.al. (2013) inferred a system that used image processing algorithm for the real time traffic light control which projected to integrate the traffic light efficiently.

Ramteke Mahesh K. et.al. (2014) proposed FPGA (Field Programmable Gate Array) controller built on Neuro-Fuzzy system thought delivered active resolution for Traffic Control. It said to used to lessen downsides of the usual traffic controllers with the precision of given difference in green cycle intervals based on the dense traffic loads that transformed at every roadways in a four leg intersection.

## III. METHODOLOGY

In this research work, the proponent utilizes the top-down design approach shown at the register-transfer level. Verilog (2019) like any other hardware description language, permits a design in either bottom-up or top-down methodology but bottom-up has to give way to the new structural and hierarchical design method which is top-down design.

### *A. Xilinx ISE Software*

As of to date, many researchers have conducted several methods for implementing the traffic control system. It can be done using a microcontroller, python, IoT and other platforms. In this case, the proponents made the innovation of the system through Verilog HDL using Xilinx ISE as the

leading software. It has the advantage over the different platforms, some of these are: it supports high-speed critical application when simulated using FPGA. It can also support a large digital circuit design [4]. Through Xilinx ISE, it allows engineers to synthesize their design, analyze RTL schematic diagrams and can conduct simulation of the design represented by waveforms [5].

### *B. Proposed System*

The system contains different signals. Under the Emergency State, system will detect incoming emergency vehicles using acoustic sensors. The siren alarm emits a particular frequency in which when it reaches higher or equal to 100 decibels, and the traffic light will be automatically turn into green color. These sensors is estimated to place in half kilometer from near intersection. Under the FIFO state, a vehicle that came first on the intersection will be moved forward.

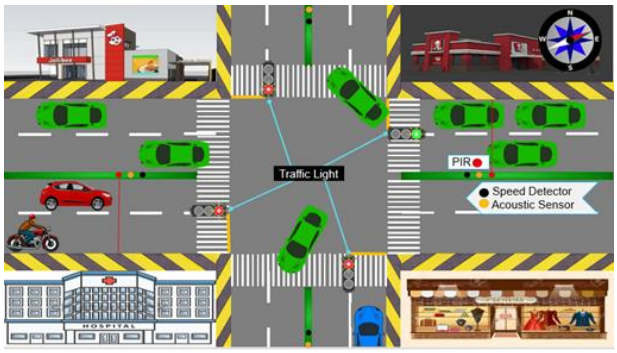


**Fig. 1.** FIFO State

Fig. 1 shown above the system consisting of three primary sensors that are essential in this project. The figure also contains local landmarks from different directions. Four traffic light are all located in every inbound lanes. The red line on every inbound lane is the PIR sensor. The PIR sensor is use for monitoring traffic flow which is the main concept for the represented figure.

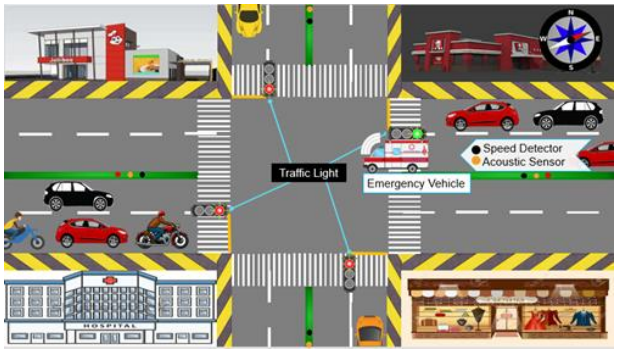


**Fig. 2.** Emergency State

Fig. 2 is shown the response of the traffic light when the emergency vehicle like ambulance is present or detected. As stated in the figure above, emergency vehicle will be treated with the utmost priority as it will save human lives.

### *C. Block Diagrma*

The block diagram shown in fig. 4 that two sensors are connected to the traffic light. These sensors will manipulate the output of traffic light based on the stated conditions. Meanwhile, TMO has the over-all accessed when it comes to monitoring.

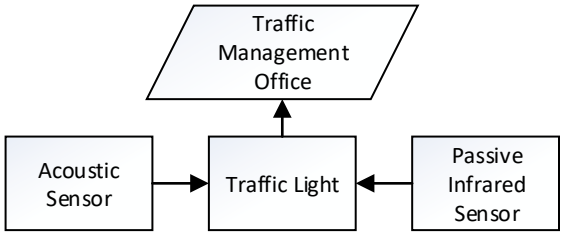


**Fig. 3.** System block diagram

### *D. IPO Chart*

Table 1 below shows the block diagram of the system in the form of IPO Chart. The inputs are the three signals that have different functions in determining the vehicle's presence and classification. The outputs will perform according to different states such as emergency state for ambulances, fire-fighter truck, police mobile and equivalent vehicle. The FIFO state uses the first-in-first-out principle.

**Table 1.** IPO CHART OF SMART TRAFFIC CONTROL SYSTEM

| Symbol | Process | Output |
|---|---|---|
| Emergency State: Acoustic Sensor | The sensor will detect the siren sound which usually greater than or equal to 100 decibels which has an up and down sound level behavior | Green traffic light will be "ON" while red color on the rest of the road. |
| FIFO State: Passive infrared sensor | The sensor will detect the traffic movement. | The traffic light will be turned into green color based on the set conditions. |

### E. Flowchart

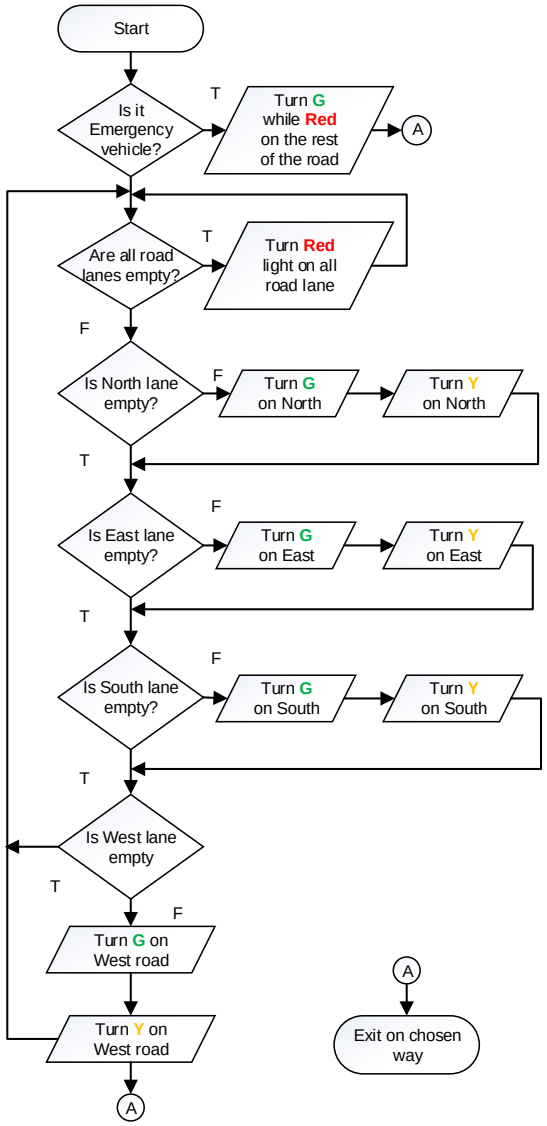


**Fig. 4.** Flowchart of SMART Traffic Control System

Fig. 4 shown above the flow chart describing the traffic algorithm cycle to aid a better understanding of the system (Osarenomase, 2015). It will start with identifying if the emergency vehicle is present then followed by a unique condition for identifying vehicle based on the first-in-first-out principle. Under this condition, if no vehicle detected near intersection, the traffic light will be on default red light status.

### F. Pseudocode

Table 2 shown below the step by step procedure of the entire system. It was constructed using readable algorithms.

**Table 2.** PROCEDURAL STATEMENT OF THE SYSTEM VIA PSEUDOCODE

| No. | Pseudocode |
|---|---|
| 1. | Start |
| 2. | Is there Emergency vehicle detected? |
| | If Yes, turn the traffic light green on that lane while simultaneously blocking the rest of the road with the color red. |
| | Otherwise, proceed to the next step. |
| 3. | Are all the road lanes empty? |
| | If Yes, turn red traffic light on all road lanes as no vehicle detected, then repeat this process. |
| | Otherwise, proceed to the next step. |
| 4. | Is North inbound lane empty? |
| | If Yes, proceed to next step. |
| | Otherwise, turn green traffic light, afterwards turn on the yellow traffic light for 3 seconds. |
| 5. | Is East inbound lane empty? |
| | If Yes, proceed to next step. |
| | Otherwise, turn green traffic light, afterwards turn the yellow traffic light on for 3 seconds. |
| 6. | Is South inbound lane empty? |
| | If Yes, proceed to the next step. |
| | Otherwise, turn green traffic light, afterwards turn on the yellow traffic light for 3 seconds. |
| 7. | Is West inbound lane empty? |
| | If Yes, go back to step 4. |
| | Otherwise, turn green traffic light, afterwards turn on the yellow traffic light for 3 seconds. |

## IV. RESULTS AND DISCUSSION

### A. Project Description

The proposed system of Smart Traffic Control System was designed through Verilog using the Xilinx ISE tool. Basically, it has two different signaling sensors that have two different processes which inclusive in one structured system.

**Table 3.** SEQUENTIAL TABLE UNDER FIFO STATE

| State | North inbound | East inbound | South inbound | West inbound | Condition Statement |
|---|---|---|---|---|---|
| C0 | R | R | R | R | All red on |
| C1 | G | R | R | R | North green |
| C2 | Y (3sec) | R | R | R | North yellow |
| C3 | R | G | R | R | East green |
| C4 | R | Y (3sec) | R | R | East yellow |
| C5 | R | R | G | R | South green |
| C6 | R | R | Y (3sec) | R | South yellow |
| C7 | R | R | R | G | West green |
| C8 | R | R | R | Y (3sec) | West yellow |

Table 3 shown above the tabular representation of traffic light green, yellow and red under FIFO state. When the green light is on, the rest of the road will stop. It is similar to one at a time green light then the yellow light will be followed just for 3 seconds to indicate that the traffic light will be changing its state into color red. Based on the table, if all the road is empty, all red traffic light will be on.

### *B. Properties of the Project*

The proponents used a simple if-else statement for this project. They also utilized the used of 19 multiplexers inside the looping statement that has been coded using case-statement. This kind of statement is good to consider when building multiple probabilities.

### *C. Functions of the System*

The system used three different sensors. The first sensor is PIR also known as passive infrared sensor. Its function is to evaluate road behavior, in particular with vehicle's movement. The sensor is focused mainly on transportation mediums e.g. cars, motors, public utility vehicle, and the like. The main purpose of PIR is for FIFO state. Second, the acoustic sensor for recognizing emergency vehicles.

### *D. Tools and Methodologies of the System*

The system was successfully coded through Verilog HDL with Xilinx ISE as for the primary tool. It allows engineers to do boundless digital design. All input sensors will process the information based on the discussed conditions.

Fig. 6 and 7 shown the top-level and low-level block of the RTL schematic diagram. It consists of six inputs: a four-bit PIR, green, red, yellow & AcousticSen. Meanwhile, the five outputs are four-bit Violator, North, East, South, West. The directions presented refers to the four traffic light positioned on every inbound lane. The Verilog source code and test bench model were both synthesized using the time scale of one microsecond over 10 nanoseconds.

A 4-bit PIR acts as a selector in the multiplexer. It is being called when the probability either cases c0 to c7 are trigger. In digital circuit, if all the sensors met certain parameters, the output will be logical '1' or logical high as shown in the fig. 8.

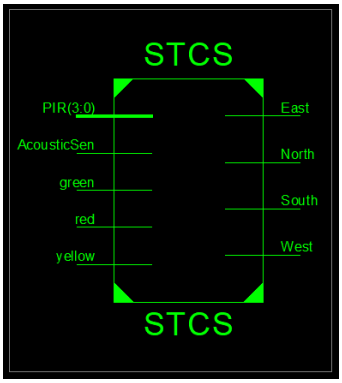


**Fig. 5.** Top-Level Block of RTL Schematic Diagram

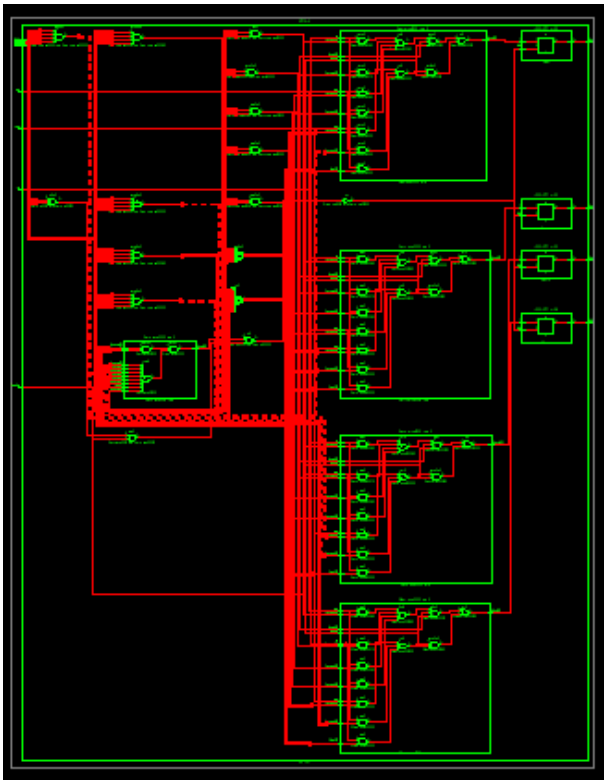

**Fig. 6.** Low-Level Block of RTL Schematic Diagram

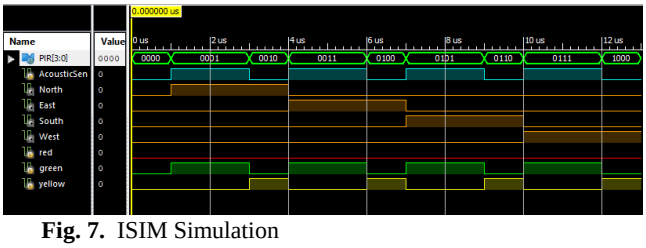


**Fig. 7.** ISIM Simulation

## V. CONCLUSION

The digital design was made successfully synthesized and verified. In particular, immediate action should be done faster when it comes to

handling human's lives. Every seconds, minutes and hour of the clock's tick matters especially when a person is dying carried by the ambulance. One of the building blocks of this designed system is the used of logic gates and multiplexers

## RECOMMENDATION

The proponents recommend adding a peak hour or rush hour analysis to whoever likely to integrate the traffic control system similar to this one. They may include a comparator of vehicles entering on intersection per hour as well as comparing the length of waiting vehicles for deeper analysis which lane should be priorities. Lastly, it would be great if the system will undergo actual testing using the FPGA board.

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